

CSD19502Q5B 80 V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

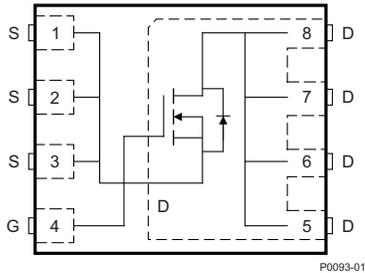
2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 3.4 mΩ, 80 V, SON 5 mm x 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	80		V
Q_g	Gate Charge Total (10 V)	48		nC
Q_{gd}	Gate Charge Gate to Drain	8.6		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}$	3.8	mΩ
		$V_{GS} = 10\text{ V}$	3.4	mΩ
$V_{GS(th)}$	Threshold Voltage	2.7		V

Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD19502Q5B	13-Inch Reel	2500	SON 5 x 6 mm Plastic Package	Tape and Reel
CSD19502Q5BT	13-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

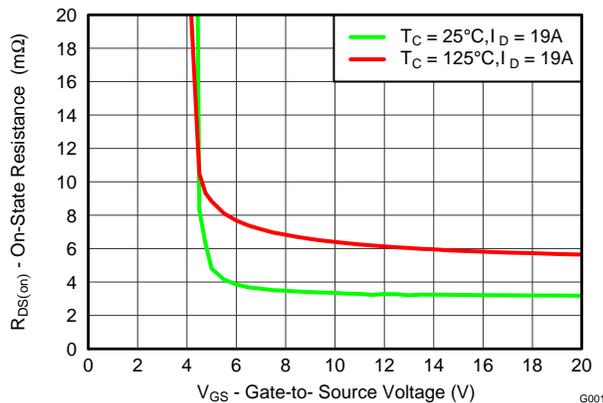
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	157	
	Continuous Drain Current ⁽¹⁾	17	
I_{DM}	Pulsed Drain Current ⁽²⁾	400	A
P_D	Power Dissipation ⁽¹⁾	3.1	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	195	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 74\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	274	mJ

(1) Typical $R_{\theta JA} = 40^\circ\text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 0.8^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$

$R_{DS(on)}$ vs V_{GS}



Gate Charge

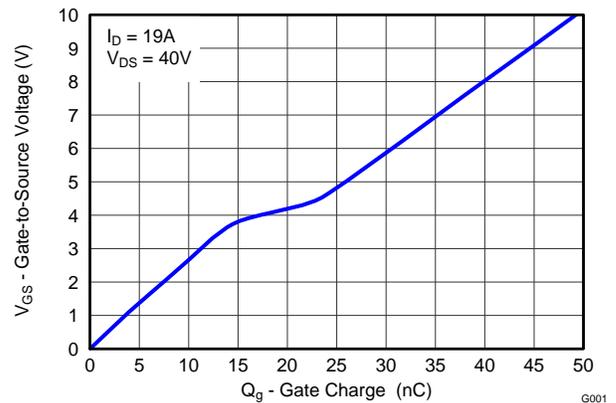


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4 Revision History

Changes from Original (December 2013) to Revision A	Page
• Added small reel option to ordering information table	1
• Increased silicon limit for continuous drain current to 157 A	1
• Increased max pulsed current to 400 A	1
• Added max power rating when the case temperature is held to 25°C	1
• Updated pulsed current conditions to specify duty cycle \leq 1%, pulse duration \leq 100 μ s, and Max $R_{\theta JC} = 0.8^{\circ}\text{C}/\text{W}$	1
• Updated Figure 10	6
• Updated mechanical drawing	9

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 64\text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.2	2.7	3.3	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}, I_D = 19\text{ A}$		3.8	4.8	m Ω
		$V_{GS} = 10\text{ V}, I_D = 19\text{ A}$		3.4	4.1	m Ω
g_{fs}	Transconductance	$V_{DS} = 8\text{ V}, I_D = 19\text{ A}$		88		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		3750	4870	pF
C_{oss}	Output Capacitance			925	1202	pF
C_{rss}	Reverse Transfer Capacitance			17	22	pF
R_G	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (10 V)	$V_{DS} = 40\text{ V}, I_D = 19\text{ A}$		48	62	nC
Q_{gd}	Gate Charge Gate to Drain			8.6		nC
Q_{gs}	Gate Charge Gate to Source			14		nC
$Q_{g(th)}$	Gate Charge at V_{th}			10		nC
Q_{oss}	Output Charge	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		130		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 40\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 19\text{ A}, R_G = 0\ \Omega$		8		ns
t_r	Rise Time			6		ns
$t_{d(off)}$	Turn Off Delay Time			22		ns
t_f	Fall Time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	$I_{SD} = 19\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 40\text{ V}, I_F = 19\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		275		nC
t_{rr}	Reverse Recovery Time			72		ns

5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

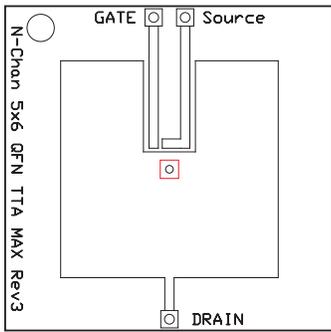
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance ⁽¹⁾			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			50	

- $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches x 1.5-inches (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

CSD19502Q5B

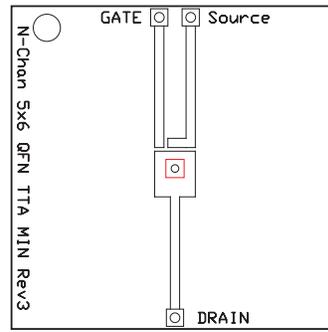
SLPS413A – DECEMBER 2013 – REVISED JUNE 2014

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M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.



M0137-02

Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

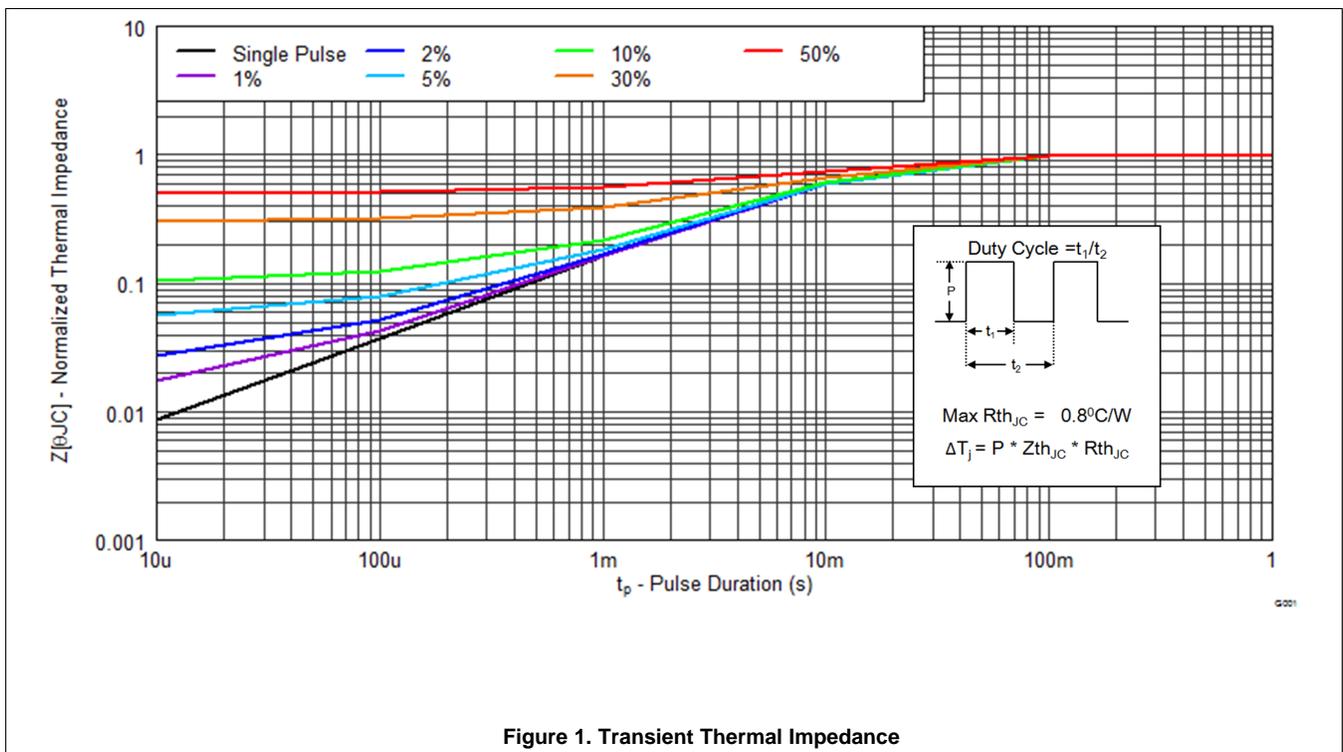


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

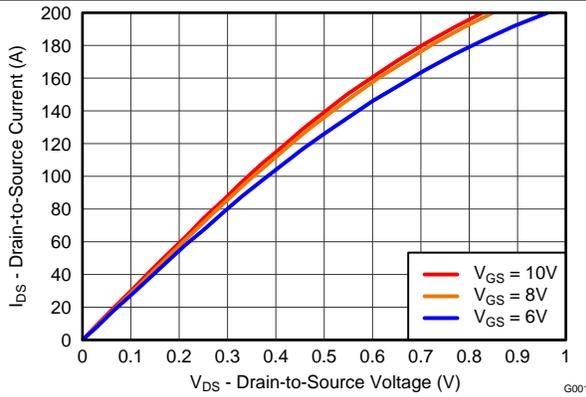


Figure 2. Saturation Characteristics

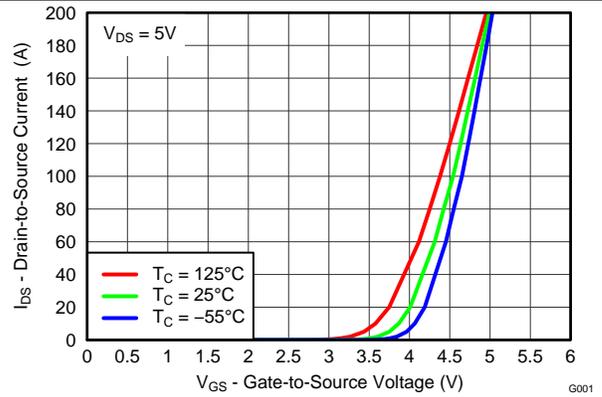


Figure 3. Transfer Characteristics

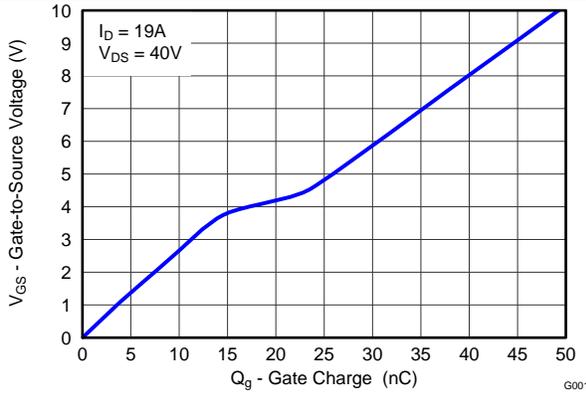


Figure 4. Gate Charge

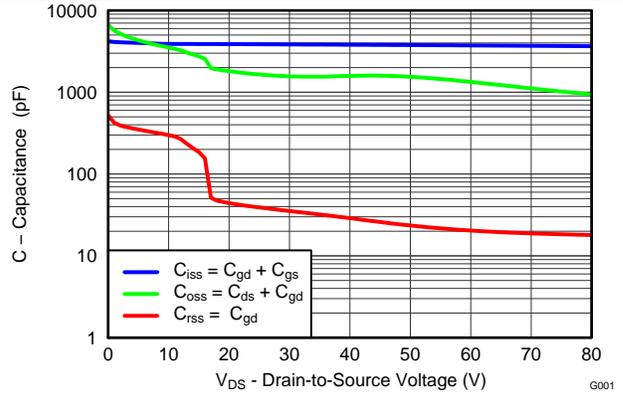


Figure 5. Capacitance

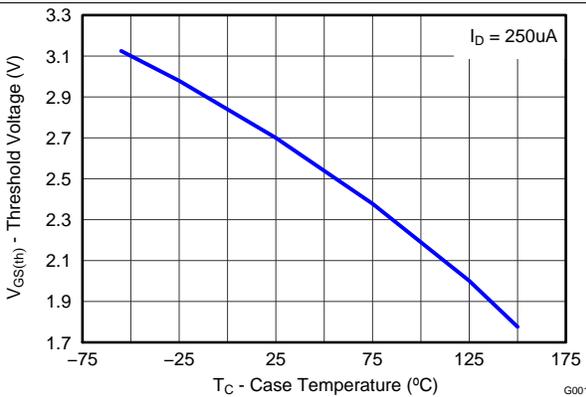


Figure 6. Threshold Voltage vs Temperature

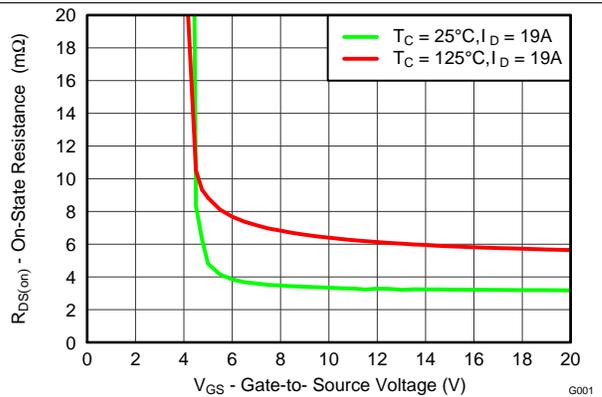


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

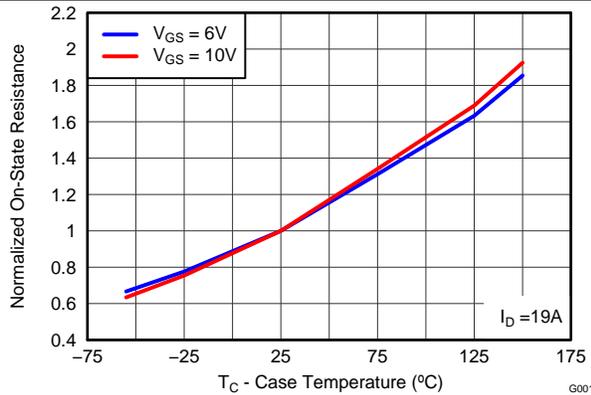


Figure 8. Normalized On-State Resistance vs Temperature

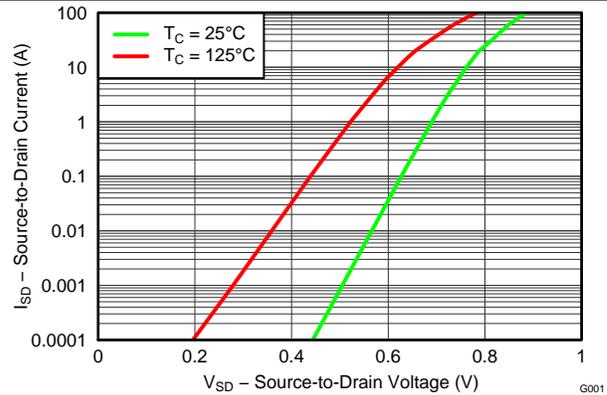


Figure 9. Typical Diode Forward Voltage

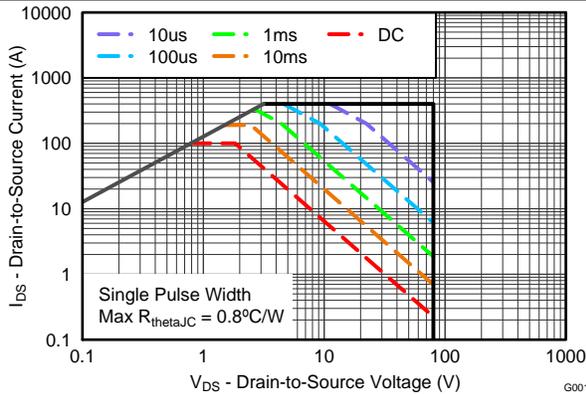


Figure 10. Maximum Safe Operating Area

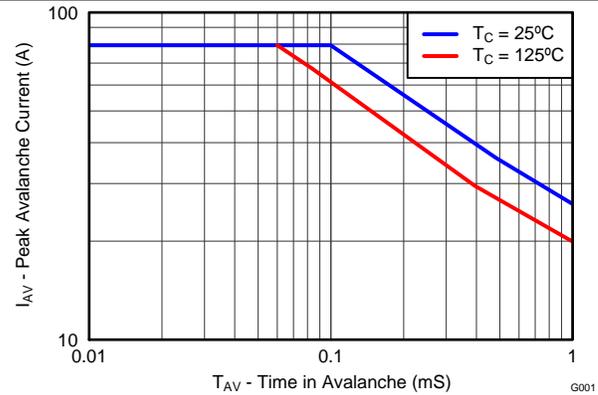


Figure 11. Single Pulse Unclamped Inductive Switching

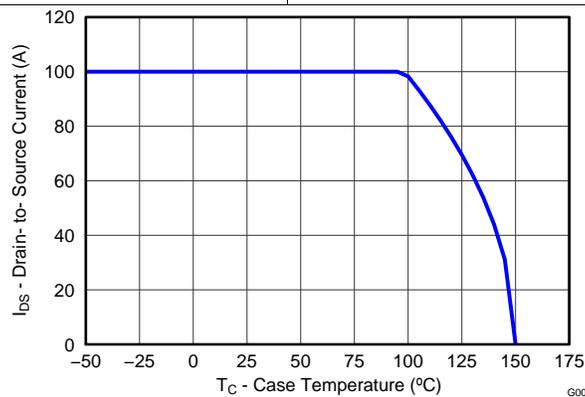


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

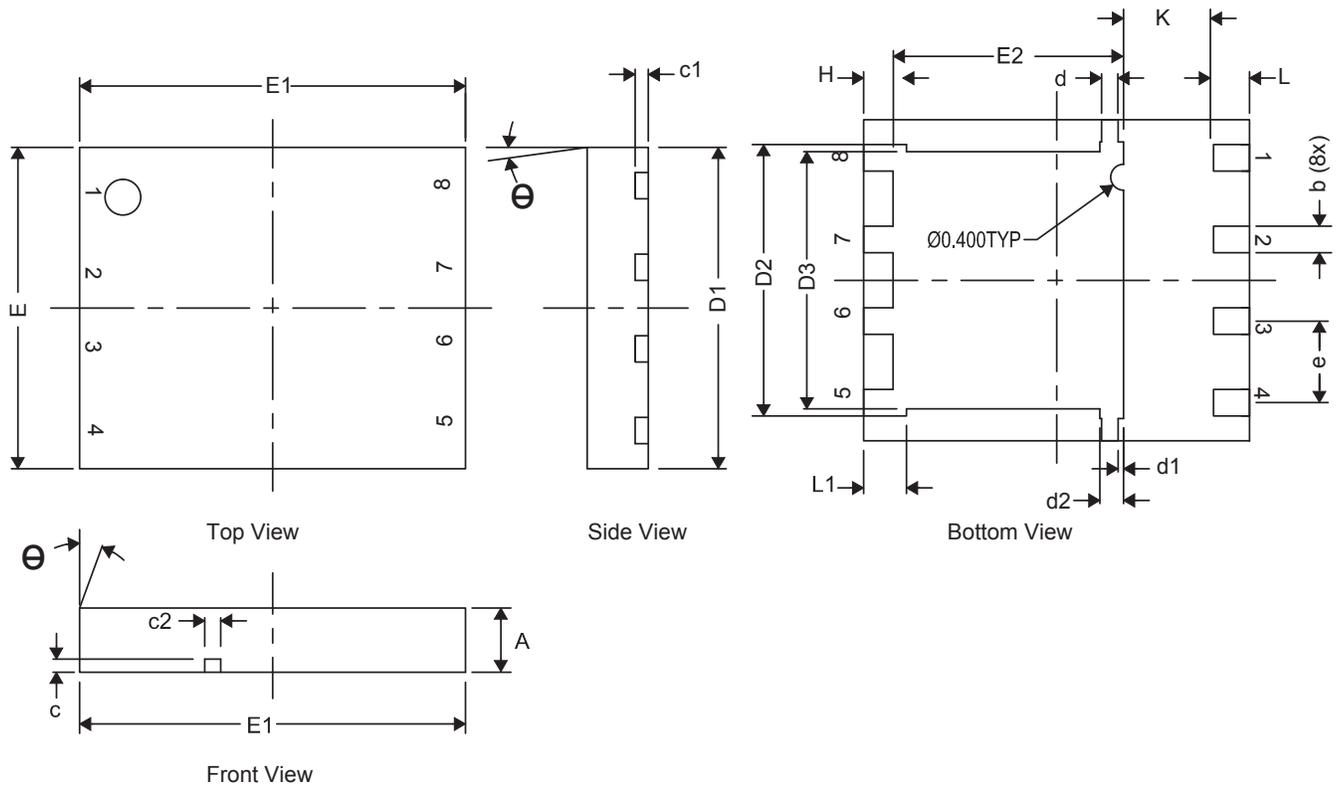
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

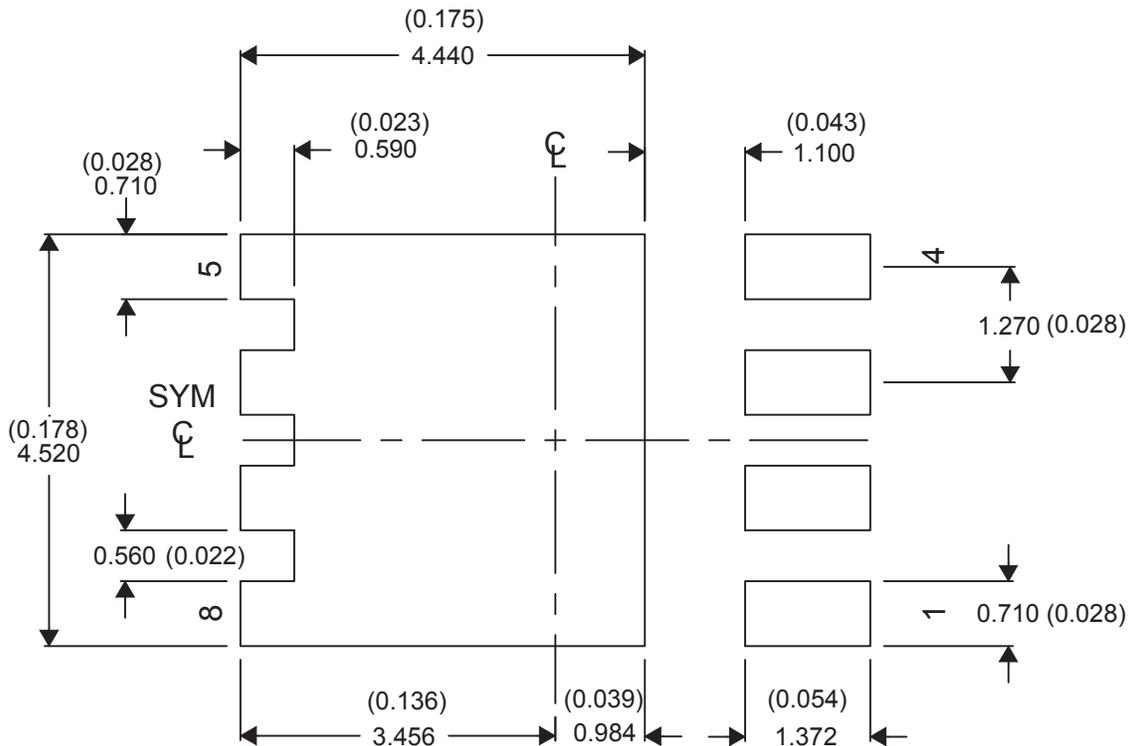
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5B Package Dimensions



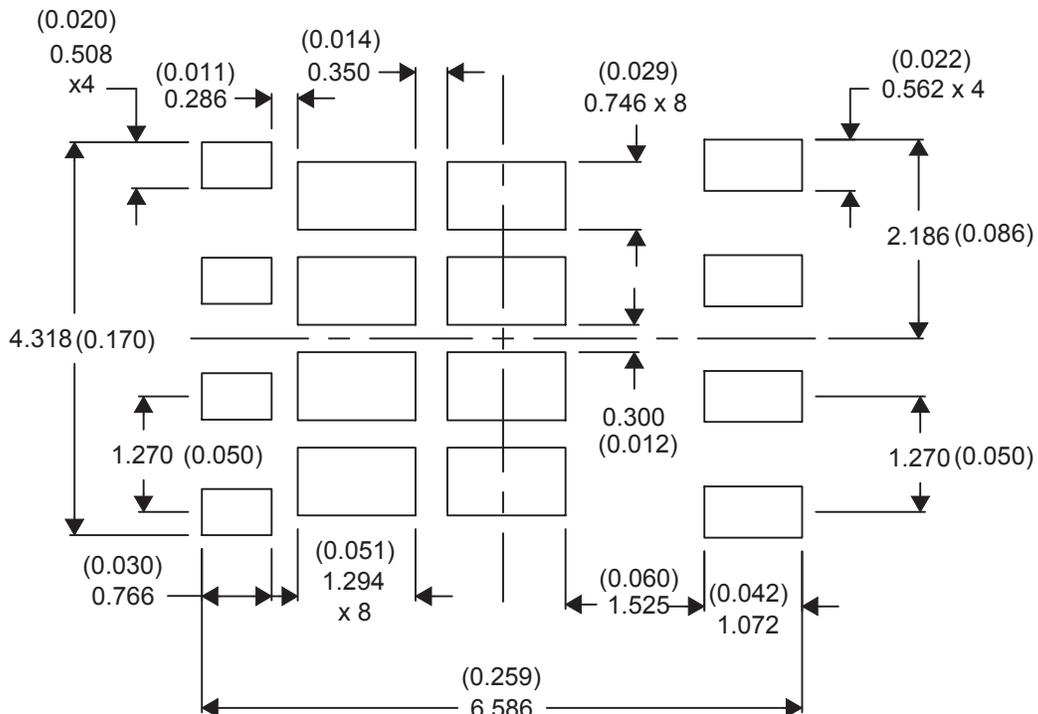
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 TYP		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 TYP		

7.2 Recommended PCB Pattern

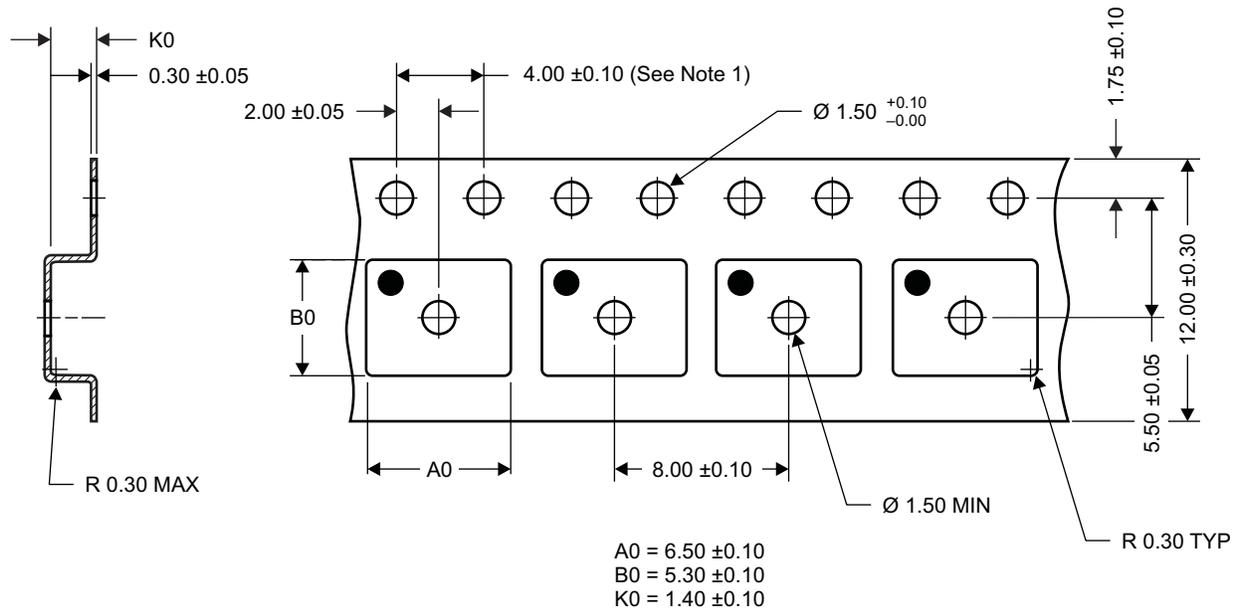


For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

7.3 Recommended Stencil Pattern



7.4 Q5B Tape and Reel Information



M0138-01

Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19502Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD19502	Samples
CSD19502Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD19502	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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